Amendments to and Listing of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for accelerating a pseudo-random input bit flow having a length of 2^{n-1} bits, generated from a polynomial of an irreducible degree n at a first clock frequency, into an identical output bit flow at a second clock frequency, greater than the first clock frequency, the method comprising:

collecting the output bit flow;

delaying the collected flow by a predetermined value (τ) respecting the following relation:

$$\tau = ((2^{\ell})*T_1)-T_0,$$

wherein T_1 represents the clock period of the input bit flow, T_0 represents the clock period of the output bit flow, and ℓ is a non-zero[[an]] integer setting a decimation parameter,

wherein delay τ is also selected to respect the following relation:

$$\tau = (2k+1)*(2^n-1)*T_0,$$

where k represents any non-zero integer, and where n represents the degree of the irreducible polynomial of the random sequence, and

combining via a recirculation loop, the delayed flow with the input bit flow ~~in a computer~~ to generate the output bit flow at the second clock frequency.

2-3. (Canceled)

4. (Currently Amended) The method of claim [[3]]1, wherein numbers k and ℓ respect the following relation:

$$(2k+1)*(2^n-1)+1 = p2^{\ell},$$

where p is the desired acceleration factor.

5. (Currently Amended) A circuit for accelerating an initial pseudo-random bit flow having a length of 2^{n-1} bits generated from a polynomial of an irreducible degree n at a first frequency, into an identical accelerated bit flow at a second frequency greater than the first clock frequency, the circuit comprising a combiner having a first input adapted to receive the initial bit flow and having an output adapted to provide the accelerated flow, a second input of the combiner being connected by a delay element to the combiner output, the delay τ of the delay element respecting the following relation:

$$\tau = ((2^{\ell})*T_1)-T_0,$$

wherein T_1 represents the clock period of the input bit flow, T_0 represents the clock period of the output bit flow, and ℓ is a non-zero[[an]] integer setting a decimation parameter,

wherein delay τ is also selected to respect the following relation:

$$\tau = (2k+1)*(2^n-1)*T_0,$$

where k represents any non-zero integer, and where n represents the degree of the irreducible polynomial of the random sequence.

6. (Previously Presented) The circuit of claim 5, further comprising a regeneration circuit configured to shape at the second frequency the output of the combiner.

7. (Previously Presented) The circuit of claim 5, wherein a phase-shifting element is further provided between the generator of the original pseudo-random bit sequence and the combiner.

8. (Previously Presented) The circuit of claim 5, wherein the initial bit flow is obtained by a flip-flop generator.

9. (Previously Presented) The circuit of claim 5, formed by at least one of optical and electronic means.

10. (Canceled)